Ballast circuit for operating a gas discharge lamp

The invention relates to a ballast circuit for operating a gas discharge lamp, comprising a half-bridge DC-AC converter having a voltage controlled oscillator for alternately switching the switches of said half-bridge, said oscillator having an input with a control voltage which determines the operating frequency of said half-bridge, a resonance circuit connected to said half-bridge for feeding the lamp, and a feedback circuit connected at one end to said resonance circuit for adjusting the operating frequency of said half- bridge.

Such a ballast circuit is described in United States Patent 5,723,953.

For igniting a (compact) fluorescent lamp two methods can be applied: warm start or cold start. Warm start means that during a specific time the electrodes are pre-heated while maintaining the lamp voltage below its ignition voltage. Because of the high electrode temperature the electrodes will start emitting electrons. When after pre-heating a lamp voltage is applied which is larger than the ignition voltage, an avalanche will take place and the fluorescent lamp will be on. As electrons are already available, the voltage across the electrodes is low during and after the ignition process, so no sputtering of the electrodes will occur, that is reflected in a high switching lifetime of the lamp.

For a cold start a high voltage is applied across the fluorescent lamp in a very short time. After ignition the electrodes needs to supply electrons to establish a lamp current. However the electrodes are cold and the only manner to generate electrons is to force them out of the electrode lattice by a high electric field. This high voltage will heat the electrode and eventually thermal emission will take place. In the time frame wherein the electrode voltage is high, the so called glow phase, sputtering of the electrode will take place that is reflected in a relatively short switching lifetime. The lamp driver should take care that the time frame wherein the electrode voltage is high is as short as possible. This means that in the glow phase maximum power should be delivered to the lamp to heat up the electrodes as quickly as possible. The lamp voltage during the glow phase is high (typically 500V, depending on the lamp type). The reason to apply the cold start mechanism is to minimize the costs of the ballast.

A lamp driver usually consists of a half-bridge topology. The pre-heating, ignition and burning states are obtained by sweeping down the frequency of the half-bridge switches over the resonance curve of the resonance (LC) network. The resonance frequency (1/(2*pi*sqrt(Llamp*Clamp)) often is chosen near the start frequency (the maximum frequency) for lowest current stress during ignition. Sweeping is often established via a voltage controlled oscillator.

For cold start the frequency sweep from the start frequency to the nominal frequency (the minimum frequency) is very short, for instance 10 ms, with respect to the glow time, which is more than 100 ms. Therefore without any measures the half-bridge will run at nominal frequency during the glow phase. Because this nominal frequency is far below the resonance frequency the half-bridge is not capable anymore of generating the high glow voltage, and furthermore the half bridge is also running in capacitive mode. As a result the lamp may extinguish, or alternatively remain in glow mode and be destroyed thereby. Known cold start lamp drivers which address this problem have non-integrated self-oscillating circuits which direct itself to resonance and thereby maximum power to the lamp in the glow phase. These circuits are however expensive and hard to integrate in an IC.

The aim of the invention is to provide a cheap and efficient integrated ballast circuit for operating a gas discharge lamp, which controls a resonant half-bridge lamp driver for maximum power during the glow phase.

Therefore the other end of said feedback circuit is connected to the input of said voltage controlled oscillator and designed such that during at least a substantial part of the start-up period of the lamp wherein the half-bridge frequency is at least nearly equal to the resonance frequency the half- bridge voltage is forced to operate at least nearly in phase with the half-bridge current. Said feedback loop thereby automatically maintains the ballast at resonance frequency, and thereby at maximum power, from the moment the frequency down sweep reaches said resonance frequency until the lamp is on.

Preferably the first end of the feedback circuit is connected to the serial connection between the two switches of the half-bridge. Also preferably said voltage controlled oscillator input is further connected to a current source and a capacitor, wherein said equilibrium is determined by said current source charging said capacitor, and said feedback circuit at least partially discharging said capacitor each half-bridge switching cycle.

The ballast circuit described herein is in particular suited to be integrated in an IC.

The invention furthermore relates to a lamp driver comprising said ballast circuit.

The invention will now be explained in more detail with respect to the drawings, which show an exemplary embodiment of the invention merely for the purpose of illustration.

Figure 1 schematically shows a conventional ballast circuit;

Figure 2 schematically shows a ballast circuit according the invention;

Figure 3 shows a time plot of a the half-bridge voltage of a ballast circuit operating in inductive mode; and

Figure 4 shows a time plot of the half-bridge voltage of a ballast circuit according the invention operating in near- resonance mode.

According to Figure 1 a typical ballast circuit for driving a gas discharge lamp comprises a DC voltage terminal (vcc) and a ground terminal (gnd), a compact fluorescent lamp, capacitors C_lamp, C_dc1, C_dc2 and C-dvdt, and a coil L_lamp. Furthermore the ballast circuit comprises a half- bridge DC-AC converter, consisting of two mosfet switches T1 and T2, which are switched by a voltage controlled oscillator VCO. The switching frequency of oscillator VCO is determined by an input voltage V_vco, wherein the frequency is highest if said input voltage is low (for instance 0 V), and lowest if said input voltage is high.

The man skilled in the art will appreciate that the resonance circuit of Figure 1 is shown for illustration purposes and may have any other suitable configuration without departing from the scope of the invention.

According to Figure 2 a feedback circuit is added to the ballast circuit of Figure 1. One end of the feedback circuit is connected to a node HB located between the two switches T1 and T2 of the half-bridge. The other end of the feedback circuit is connected to the control voltage input of the voltage controlled oscillator VCO. The feedback circuit comprises capacitors C_sense, a switch T4 and a transistor T3. T2 and T4 are coupled such that T4 is on if T2 is off, and vice versa.

The frequency down sweep of the voltage controlled oscillator VCO is achieved by a current source J_0 and capacitor C_sweep, in between which the VCO input is connected. When the ballast is switched on the current source J_0 starts to load capacitor

C_sweep and thereby the control voltage V_vco rises while the switching frequency of the VCO goes down, thereby approaching the resonance frequency of the resonance circuit. As long as the operating frequency is (much) higher than the resonance frequency the resonance circuit is operating in inductive mode, as reflected in Figure 3. In that case the voltage across T2 is zero when T2 is switched on.

However, near resonance the phase angle between the half- bridge current and the half-bridge voltage becomes so small that, given a fixed dead time DT, wherein both T1 and T2 are off, the half-bridge voltage starts to swing back during the dead time, as shown in Figure 4. Therefore, when T2 is switched on there is a negative voltage step VHard at the half-bridge node HB. This results in discharging C_sweep via T3 and C_sense, and thereby a lower control voltage V_vco and a higher operating frequency.

These two opposite forces, i.e. the charging of C_sweep by current source J_0 and the partial discharging of C_sweep when T2 is switched on, forces the ballast towards an equilibrium wherein V-vco remains constant, and thus the ballast operates at near-resonance frequency wherein the half-bridge current and the half-bridge voltage are (nearly) in phase and maximum power is fed to the lamp until the lamp is on.

The amount of charge involved in the discharging of C_sweep equals Vhard * C_sense. The equilibrium thus exists when:

$$(J\_0 * T) - (Vhard * C\_sense) = 0$$

Given the frequency $f = 1/T$, Vhard can be expressed as follows:

$$Vhard = J\_0/(f * C\_sense)$$

For example, if $J\_0 = 250$ nA, $f = 50$ kHz and C_sense = 330 fF, then Vhard = 15 V. So the system controls itself so close to resonance that just before switching on the lowside / highside power the drain source voltage equals 15 V. Thus no dedicated control loop is necessary.